

# VHDL Tools

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## 1 ModelSim

Producer: Model Technology Inc.  
Homepage: <http://www.model.com>  
Latest release: 5.6

### 1.1 Introduction

Professional robust software offering wide possibilities in VHDL and Verilog simulation. It features high speed and target hardware platform adaptability.

### 1.2 Licensing

#### 1.2.1 Commercial

The basic commercial versions are *ModelSim PE* and *ModelSim SE*, their comparison is available at: <http://www.model.com/products/prodcomp.asp>. Software can be downloaded from <http://www.model.com> or you can use a direct download link: <http://www.model.com/products/release.asp> (from this page, full versions can be downloaded and a link to evaluation versions is also included). There are two licensing options for paid full version:

- Licensing file is located on a server which is connected to the Internet; then it is possible to work on a remote machine referencing the license file on the server (it is necessary to be connected to the Internet while using *ModelSim*).
- Hardware key attached to a standalone machine along with a license file on it's hard drive; these steps should be followed (in Windows):
  1. Install *ModelSim PE* from CD and choose the proper type of HW key during the installation (picture is provided)
  2. Connect the HW key

3. Set up environment variable *LM\_LICENSE\_FILE* pointing the license file location, i.e.:  
SET LM\_LICENSE\_FILE= C:\FLEX1m\license.dat (this line is added into *autoexec.bat*)
4. Install *Mentor Graphics Licensing* from CD 2 FPGA Advantage and enter the path to the license file when prompted
5. Restart computer
6. Run *ModelSim*

The manufacturer charges a fee for server changes and/or licence transfers. A month evaluation licence can be requested:

- Memory limited version (7MB) – for *Microsoft Windows* only (the license can be requested using a web form or e-mail, the instructions are given during the installation process; the license file is sent via email as an attachment).
- Unlimited version – (a sales representative must be contacted in order to request this license) Warning! Evaluation Licences are not given to educational institutions. Therefore, obtaining a license depends on the type of business entered in the evaluation request. The installation file of the evaluation version can be used not only to install the evaluation version, but to install a full version as well. This choice is made in the beginning of the installation process. Subsequently, an appropriate license file is required.

### **1.2.2 Working with the license file**

The linkage between the *ModelSim* and its license file is provided by *Licensing Wizard*, which is installed along with *ModelSim* (in *Microsoft Windows*, there is a shortcut in the *ModelSim* program group). Principally, one of two different approaches can be chosen: licence from a remote server (paid version) or local licence (paid or evaluation version). If the licence is local, the user simply enters the path to the license file on a local hard drive. In the other case, the same dialog box is used to enter a string which should look this way: *port@server.address* (default port number is 1650, the Merlot server uses port number 1717 and therefore we would write *1717@merlot.ics.muni.cz*). The program will automatically make a correct setup of environment variables. When using *Microsoft Windows 98* or *Millennium edition* a restart is needed to complete the procedure.

#### **ModelSim SE**

– Operating system: *UNIX (Sun Solaris, IBM AIX, HP-UX), Linux (Redhat 6.0 - 7.2)*,

*Microsoft Windows (98, Me, 2000, NT, XP)*

– Available version: 5.6

### **ModelSim PE**

– Operating system: *Microsoft Windows (98, Me, 2000, NT, XP)*

– Available version: 5.6

### **1.2.3 Free**

#### **ModelSim XE**

– Operating system: *Microsoft Windows* (applicable for the whole Webpack)

– Available version: 5.5

It is possible to gain *Xilinx Webpack* for free at <http://www.xilinx.com>. At first, it is necessary to create a Xilinx.com account, this can be made at [http://www.xilinx.com/xlnx/xil\\_reg\\_prof](http://www.xilinx.com/xlnx/xil_reg_prof). Furthermore, a registration extension must be done in order to be able to download software. The best way to do this is going to this web page: [http://www.xilinx.com/xlnx/xil\\_prodcat\\_landingpage.jsp?title=ISE+WebPack](http://www.xilinx.com/xlnx/xil_prodcat_landingpage.jsp?title=ISE+WebPack) This page is devoted to the *Webpack* and includes a link to desired downloads as well. The main application of this pack is the *Project Navigator*; it is an application providing access to all stages of a VHDL design (compilation, synthesis, place and routing) and enables different-levels simulation. *ModelSim XE* is used for simulation, this version of *ModelSim* is included in the *Webpack* and therefore it is free. However, the downloads and installations of *ModelSim* and the *Webpack* itself are separate and independent: it is necessary to download two files and install both of them to get full functionality of the *Webpack*. *ModelSim* can be integrated into the *Project Navigator* after finishing both installations by clicking menu *Edit - Preferences - Partner Tools* in the *Project Navigator*. Prior to the first use of the *ModelSim*, a *ModelSim XE STARTER license* must be obtained. The request is performed using the web interface; the “Submit license request” shortcut in the *ModelSim XE* program group can be used. The form is pre-filled according to the data previously submitted when creating the Xilinx.com account and therefore just confirmation is needed. The licence is delivered via e-mail instantly; the license file is handled in the same way as mentioned above describing commercial versions.

Notes:

1. Neither type of applicant’s business nor membership in Xilinx University program matters when acquiring the licence.
2. *Webpack* can cooperate with commercial versions of *ModelSim* as well.

3. *Webpack* includes an own simulation tool called *HDL Bench* which can be used either.

### 1.3 Interesting add-on

*Debug Detective*: This tool enables displaying any part of a design in the form of a state or block diagram, graphical breakpoints, cross linkage between graphical breakpoints and the source code, cause analysis and more. This add-on is sold separately (it is not even in *ModelSim SE*); more information is available at <http://www.mentor.com/hdl/designer/debugdetective/>

### 1.4 Operating, usability

*ModelSim* features tabular operating and on the whole, it looks smarter than i.e. *Aldec Active-HDL* (see below). On the other hand, it is usually necessary to work with several windows simultaneously (the main program, waveform, source code), and that is not too comfortable. It is possible to use *ModelSim* on screens with lower resolutions; program windows are simple and pragmatic. Overall stability is very good.

Usability for simulation is excellent. This rating is based on using all described versions of *ModelSim*.

## 2 Aldec Active-HDL

Producer: Aldec

Homepage: <http://www.aldec.com>

Contact: [info@aldec.com](mailto:info@aldec.com);

[http://www.aldec.com/ContactUs/IntDistributors/distributors\\_EasternCentralEurope.htm](http://www.aldec.com/ContactUs/IntDistributors/distributors_EasternCentralEurope.htm)

Latest release: 5.1

### 2.1 Introduction

*Active-HDL* is a commercial software, fully comparable with *ModelSim*. It includes *Block diagram editor*, *State diagram editor* and system libraries (Xilinx is also supported).

### 2.2 Licencing

#### 1. Full version

- Operating system: *Microsoft Windows (98/Me, NT, 2000 and XP)*
- Available version: 5.1 PE (Plus Edition), SE (Standard Edition) or EE

(Expert Edition)

for details see [http://www.aldec.com/ActiveHDL/AHDL\\_51/51\\_Configuration\\_list.pdf](http://www.aldec.com/ActiveHDL/AHDL_51/51_Configuration_list.pdf)

## 2. Evaluating version

– Operating system: *Microsoft Windows*

– Available version: 5.1

Aldec offers this fully functional 20 days copy with the following limitations:

- Printing is disabled
- The maximum simulation time is 10 us
- The maximum size of source file being compiled is 5KB
- The maximum amount of memory allocated per VHDL, Verilog or mixed VHDL-Verilog design is 5MB. This simulation decreases to 2MB for any designs employing Edif-based designs units
- Block diagrams containing more than 15 fubs and/or symbols cannot be saved.

You can download this program (singlefile 57MB) after registration. Program is then ready to be used. Or you can skip the registration process and use this link:

[http://www.aldec.com/Registration/AHDL51\\_main\\_webeval.htm](http://www.aldec.com/Registration/AHDL51_main_webeval.htm) A 10-days unlimited license of *Active-HDL* can be obtained by contacting Aldec at the link as above.

## 3. Student edition

– Operating system: *Microsoft Windows*

– Available version: 4.2

– Price: 59.95 USD + 12.75 USD (international shipping fee for each copy)

– Order: [http://www.aldec.com/ActiveHDL/university\\_Studentedition.htm](http://www.aldec.com/ActiveHDL/university_Studentedition.htm)

This edition contains: *Waveform Viewer, HDL Editor, Block Diagram Editor*, VHDL or Verilog simulation up to 50 us, source files up to 10 KB. Only the sample designs shipped with the software can be accessed and new designs with the following names can only be created: Design1, Design2, Design3, . . . Design9. The compiler cannot compile source files larger than 10 KB. *Metamor VHDL Logic Compiler* is disabled. The *Testbench Wizard* is disabled. Simulation time is limited to 50 us. Each design is limited to a maximum amount of 10 MB of memory. The *Waveform Editor* is a viewer only – editing capabilities have been disabled. A single Block Diagram sheet cannot contain more than 7 symbols and/or fubs. Running in Batch Mode has been disabled. For more information see

#### 4. University program

- Operating system: *Microsoft Windows*
- Available version: 5.1

This is an educational version of Aldec's commercially available software and there are no feature limitations on the software, but it may only be used for educational purposes within an accredited university lab.

##### **Licensing:**

- Network License – price: 185 USD per year + 20 USD per year for each license (version SE).

For more information see:

[http://www.aldec.com/ActiveHDL/university\\_Network.htm](http://www.aldec.com/ActiveHDL/university_Network.htm)

- Hardware key – Educational keylocks can be purchased as a single seat (1) or in units of (5) each seat includes a keylock.

Price: 2200 USD for 5 licences for 3 years (version SE)

[http://www.aldec.com/ActiveHDL/university\\_Bundles.htm](http://www.aldec.com/ActiveHDL/university_Bundles.htm)

### 2.3 Program features

**HDL Editor:** is tightly integrated with the compiler and simulator. The editor features, among others: Keyword coloring for VHDL, Verilog, and C/C++. Easy-to-access context-sensitive help on VHDL and Verilog syntax. Bookmarks, hyperlinks to files and URLs. Also automatic indenting of edited code according to VHDL and Verilog syntax. Automatic division of source code into groups according to the VHDL and Verilog syntax.

**Block Diagram Editor:** a tool for graphical entry of VHDL, Verilog and EDIF designs. It can be automatically converted into structural VHDL, Verilog or EDIF netlist. The *Code2Graphics* converter is a tool designed for automatic translation of VHDL or Verilog source code into *Active-HDL* block and state diagrams.

**The Waveform Viewer:** a tool designed to display simulation results in the form of graphical waveforms.

**Design Browser:** a tool designed for management of the resources of the current design.

**Language Assistant:** a tool designed to help you develop VHDL and Verilog source code.

## 2.4 Operating, usability

According to my experiences with *Aldec Active-HDL*, it provides the same functions as *ModelSim*. Program supports these standards: VHDL, Verilog, Verilog, EDIF, Waves and Active-HDL Macro Language. I like the visual interface of this program, everything is placed into one single window. Changing between each window is done by bookmarks (compared to *ModelSim* it is much more comfortable). But using this program might seem little bit confusing—many buttons, some of them are useless (for example: a button which changes bookmark is placed in the same group as button for viewing/hidding panels). Thus the idea to put everything into one window it is necessary to set higher resolution (1024x768). Zoom-in function is limited in the *Waveform* too (in *ModelSim* it is not). Software shows certain signs of weakness: some actions (for example *Run Until*) are executed despite of pressing *Cancel* button in dialog window. The stability of program is similar to *ModelSim*'s stability (more likely to be average). My experience with simulation are very good. The biggest advantage of this program is amount of functions and features.

## 3 Xilinx Webpack

Producer: Xilinx

Homepage: <http://www.xilinx.com>

Operating system: *Microsoft Windows* (applicable for the whole Webpack)

### 3.1 Introduction

For further information about installation see *ModelSim XE* section. The process of obtaining the installation file is the same. Central application is *Project Navigator* that handles whole process of VHDL design (compilation, synthesis, place and routing).

### 3.2 Main features

#### Design entry

- *HDL editor* – includes syntax coloring feature which supports these three languages: VHDL, ABEL and Verilog
- *StateCAD Machine editor* – tool for creating and editing finite state machine designs

- *Schematic editor* – graphical tool used to capture particular electronic circuits. These schematic can be used solely for documentation.
- *Floorplanner* – an interactive graphical tool that allows you to view and edit constraints (routing, timing, grouping, initialization, synthesis, mapping and placement constraints) in your design.

**Synthesis** – XST (Xilinx synthesis Technology)

### **Simulation**

You can either use *ModelSim* (see section 1.2) or *HDL Bencher* which is a part of *Webpack*.

Implementation

- *Timing Anylyzer* – way to perform static timing analysis on FPGA and CPLD designs
- *XPower* – post-route analysis tool
- *Chipviewer*

Programming

- *iMPACT* – configuration tool, allows you to configure your PLD designs
- *PROM File Formatter* – Formats BIT files into a PROM file that is compatible with Xilinx and third-party PROM programmers, concatenate multiple bitstreams into a single PROM file for daisy chain applications and store several applications in the same PROM file (using the Xilinx FPGA reconfiguration capability)

## **3.3 Operating, usability**

*Project Navigator* allows you to manage your project files. The screen is very well arranged, it is divided into several parts. Thus it is not necessary to use several windows simultaneously.

## **4 FPGA Advantage**

Available version: 5.2

Operating system: *HP-UX 10.20/11.0, Solaris 7/8, Microsoft Windows 98/Me/2000/NT*

Producer: Mentor graphics

## 4.1 Introduction

Commercial software. The main application of this software pack is called Design Browser; it is a graphical environment covering the whole process of a VHDL design (organizing files, design creation, compilation, synthesis, place & routing).

## 4.2 Main components

- ModelSim for simulation
- Leonardo Spectrum for place & routing
- The main application is Design Browser. It's desktop is divided into several windows:
  - Source: contains textual and graphical source data
  - HDL: generated code
  - Side data: shows data associated with items selected in Source window
  - Downstream: contains data for ModelSim and Leonardo Spectrum

## 4.3 Operating, usability

HDL2graphics function is supported. Overall, block diagram creation and handling is supported at a high level of usability and comfort. FPGA Advantage provides lots of functions and it is not very simple to get orientated despite controlling's being quite well structured. ModelSim integration is very good.

# 5 VHDL Studio

Producer: Green Mountain Computing Systems, Inc.

Homepage: <http://www.gmvhdl.com>

Operating system: *Linux, Microsoft Windows, Solaris*

## 5.1 Introduction

A commercial software, which is meant to offer strong functionality in simulation. But when you compare it to it's competitors, *VHDL Studio* seems to be the worse one.

## 5.2 Licensing

1. 14 days evaluating version
2. Full version – price: \$1595

## 5.3 Program features

- Project Manager
- VHDL editor (highlighting, syntax errors detection)
- State Machine editor
- Component Creator (creates graphical component from entity)
- Graphical Testbench Designer

## 5.4 Operating, usability

Program looks well arranged and simple. Using it is very easy, but whole user interface seems to be quite chaotic (menu, source files, libraries, packages, waveforms). There is no command line which is an essential problem. We have not figured out how to change a value of variable while simulation is running (force function in *ModelSim*). The Help is not very rich. There are some bucks in functions and features, mainly in simulation. Apparently *VHDL Studio* is not very sophisticated program, and I think not proper for our purposes.

# 6 DK1

Producer: Celoxica

Homepage: <http://www.celoxica.com>

Operating system: *Microsoft Windows (98, 2000, NT 4.0, XP), Solaris, Linux*

Price: \$35,000

## 6.1 Licensing

1. Full version
2. Evaluating version – only *Microsoft Windows*  
This restricted version of the *DK design suite* is available, free of charge to authorized users, for a time-limited period of 30-days only.

### 3. Academic edition

Contains *DK Learning Series* (Computer Based Training Module) and *DK Design Suite Academic Edition*. Registration is required by sending e-mail with full address to [uniprogram@celoxica.com](mailto:uniprogram@celoxica.com)

*Handel-C* language has been designed to describe software algorithms which are directly compiled to hardware. It is based on *ISO/ANSI-C* extended to support flexible data widths, parallelism and communications/synchronization between parallel threads. The *Handel-C* language is built around a very simple timing model. The compiler generates architecture optimized EDIF netlist ready for input to FPGA and PLD place and route tools.

The built-in co-simulation feature facilitates co-design with instruction set simulators (such as *ModelSim*) and external C/C++ test benches.

*DK1* supports *Xilinx Virtex-II Pro*

## 7 CoCentric SystemC HDL CoSim

Producer: Synopsis

Homepage: <http://www.synopsis.com>

Price: \$26,950

*CoCentric SystemC HDL CoSim* is a software tool that generates the interface and allows for co-simulation of designs that are a mix of *SystemC* modules and hardware description language (HDL) Verilog modules or VHDL entities. Designers can then use the most appropriate modeling language for each part of the system to verify design correctness.

Program generates wrappers for *SystemC* modules, Verilog modules and VHDL entities, which provides a communication interface between the *SystemC* module and the HDL entity-under-test for co-simulation.

-Import mode(HDL entity-under-test into a *SystemC* environment)

-Export mode(*SystemC* module into and HDL environment)

*SystemC* class library is available from the Open SystemC Initiative web page at <http://www.systemc.org>